the present invention. As shown in Fig. 1, the sawtooth wave generating apparatus 1 of the present invention includes a base frequency generating section 10, a frequency generating section 20, a sawtooth wave forming section 30, a sawtooth wave discharging pulse circuit 40, an amplifier 50, a voltage comparator 60, a phase comparator 70, and a low-pass filter (LPF) 80. Further, the sawtooth wave generating apparatus 1 includes a digital-analog converter (DAC) 91, and a central processing unit (CPU) 90 connected to the DAC 91, the base frequency generating section 10 and the frequency generating section 20 for controlling them. A detailed description of each component is given below with reference to Figs. 2-5.

The base frequency generating section 10 is shown as a phase lock loop (PLL) circuit including a crystal oscillator in the present embodiment. However, the present invention is not limited to this structure, but a PLL circuit using other oscillator may be utilized if the oscillating frequency thereof is stable. Further, in the case where the reference frequency undergoes a change due to disturbance or the like, the sawtooth wave generating apparatus 1 can be utilized effectively because it can outputs a stable sawtooth wave.

Fig. 2 is a block diagram schematically illustrating a base frequency generating section 10 in the sawtooth wave generating apparatus 1 shown in Fig. 1. As shown in Fig. 2, the base frequency generating section 10 includes a crystal oscillator 101, a reference frequency generating section 102, 1/M divider 103, a phase comparator 104, an LPF 105, a voltage controlled oscillator (VCO) 106, and 1/N divider 107. The values M, N that are respectively dividing ratios of the 1/M divider 103 and 1/N divider 107 are controlled by the CPU 90. In this way, the base frequency generating section 10 generates a signal having a desired base frequency by appropriately changing the dividing ratios M, N of two dividers 103, 107, and outputs the signal to the frequency generating section 20.

Namely, a predetermined frequency of the signal outputted from the reference frequency generating section 102 based on the oscillating frequency of the crystal oscillator 101 is divided into 1/M by means of the 1/M divider 103 to input the divided signal to one input terminal of the phase comparator 104. The output signal from the base frequency generating section 10, i.e., the output signal from the VCO 106 is inputted to the 1/N divider 107 through a feedback loop, and the output signal from the VCO 106 that undergoes 1/N dividing operation by the 1/N divider 107 is inputted to another input terminal of the phase comparator 104.

The phase comparator 104 compares the phases (i.e., frequencies) of the two input signal mentioned above to output a comparison signal (comparing result) to the LPF 105. The VCO 106 adjusts the output signal based on the comparison signal whose high frequency component is cut out by the LPF 105, and finally the signal having the frequency as N/M times as the frequency of the signal generated in the reference frequency generating section 102 is outputted to the frequency generating section 20.

Fig. 3 is a block diagram schematically illustrating the frequency generating section 20 in the sawtooth wave generating apparatus 1 shown in Fig. 1. As shown in Fig. 3, the frequency generating section 20 includes an H period forming section 201 and an L period forming section 202. Each of the H and L period forming sections 201, 202 is controlled by the CPU 90. Thus, the frequency generating section 20 outputs a reference signal having a predetermined frequency to one input terminal of the phase comparator 70. As seen from Figs. 6 and 7, the reference signal is a square-wave which alternately assumes two fixed values (i.e., high level and low level).

Here, A description will be given for a resonant frequency characteristic in the case of using a piezoelectric element having a piezoelectric effect as a load. Fig. 8 is a graph illustrating a resonant frequency characteristic of a piezoelectric element. As shown in Fig. 8, the piezoelectric element utilized as the load

has a resonant point (i.e., resonant frequency fc) within a resonant frequency region. The resonant point depends on physical conditions such as a shape of a rotor, a wearing state of the rotor, humidity, load characteristic, or the like in the driving device with a piezoelectric element whose resonant frequency constantly undergoes a change.

In this regard, in the case where the sawtooth wave generating apparatus 1 of the present invention drives a piezoelectric element as a load, the sawtooth wave generating apparatus 1 must change the frequency of the reference signal outputted from the above-mentioned base frequency generating section 10 in response to the variation of the resonant frequency. Because the sawtooth wave generating apparatus 1 cannot carry out the PWM control accurately if the frequency of the drive signal for controlling the piezoelectric element, i.e., the resonant frequency shown in Fig. 8 does not correspond with the frequency of the sawtooth wave output signal that is an output signal from the sawtooth wave generating apparatus 1. In this case, when the CPU 90 receives the signal indicating that the resonant frequency of the piezoelectric element undergoes a change, the CPU 90 adjusts the frequency of the output signal from the base frequency generating section 10 by appropriately changing the dividing rate(s) of the 1/M divider 103 and/or 1/N divider 107 in the base frequency generating section 10.

In this way, the sawtooth wave generating apparatus 1 of the present invention can arbitrarily set the frequency of the drive signal by changing the frequency of the output signal from the base frequency generating section 10 in response to the variation of the resonant frequency of the load (i.e., piezoelectric load), and changing the H period and L period of the frequency generating section 20 by control of the CPU 90.

Fig. 4 is a block diagram schematically illustrating a sawtooth wave forming section 30 in the sawtooth wave generating apparatus 1 shown in Fig. 1. As shown in Fig. 4, the sawtooth wave

forming section 30 includes a first field-effect transistor (FET) 301, a second field-effect transistor (FET) 302, a resistor 303, a capacitor 304, an insulated gate FET (IGFET) 305 that is a semiconductor device, and a voltage source (ideal) 306.

A gate electrode of the first FET 301 is connected to the output side of the LPF 80, and a source and drain electrodes of the first FET 301 are respectively connected to a source electrode of the second FET 302 and the voltage source 306.

A gate electrode of the second FET 302 is connected to the drain electrode of the first FET 301 and the voltage source 306. A drain electrode of the second FET 302 is connected to one terminal of the resistor 303 and one conducting surface of the capacitor 304. The drain electrode of the second FET 302 is also connected to the amplifier 50. Further, the other terminal of the resistor 303 is connected to one terminal of the IGFET 305, and both the other conducting surface of the capacitor 304 and the other terminal of the IGFET 305 are connected to ground.

The first and second FETs 301, 302, and the constant voltage source 306 constitute a constant current circuit 310 that outputs a current I_D having a predetermined constant current value in response to the output signal from the LPF 80. The constant current circuit 310 can control the amount of the output current I_D by changing the amount of the drain current of the second FET 302 within the range less than the maximum value of the drain current of the second FET 302, which is determined by the voltage applied from the voltage source 306, based on the output signal (voltage value) from the LPF 80. In the present embodiment, the output signal from the LPF 80 may be regarded as a control signal of a current control device (not shown) for controlling the amount of the output current from the constant current circuit 310. In this case, the current I_D outputted from the constant current circuit 310 can be controlled using this control signal. In the case where the output signal from the LPF 80 is a high level, the voltage applied to the gate electrode of the first FET 301 is increased according to the